REMARKS/ARGUMENTS

1. Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

The amendments made to the claims in the above section are over the last entered amendment filed February 24, 2005.

2. Rejection of claims 1-26 under 35 U.S.C. 102(b):

Claims 1-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Pour (US 6,335,564) for reasons of record, as recited on pages 2-3 of the above-indicated Office action.

Response:

The applicant has amended claims 11 and 19 to overcome this rejection. Claims 1-10, 12-18, and 20-26 have been cancelled, and are no longer in need of consideration. Claims 11 and 19 now each contain the limitations of "a first lead frame connected to a second bonding pad through a first pin of the chip" and "a second lead frame connected to a third bonding pad through a second pin of the chip for receiving input signals to control the voltage level of the second pin". These limitations are supported by Fig.6 and paragraphs [0021] and [0022] of the instant application. No new matter is added through these claim amendments.

On the other hand, Pour does not teach receiving input signals through a second lead frame for controlling the voltage level of the second pin. Therefore, currently amended claims 11 and 19 are patentably distinct from the cited prior art, and reconsideration of claims 11 and 19 is respectfully requested.

3. Introduction to new claims 27-32:

New claims 27 and 30 are new apparatus and method claims, respectively. These claims are based on currently amended claims 11 and 19, and also contain the limitations of "a package substrate connected to either a high voltage or a low voltage" and "the first lead frame being connected to either a high voltage or a low voltage, and the voltage level of the first pin being the logical opposite of the voltage level of the package substrate". These amendments are fully supported by paragraphs [0021] and [0022] of the instant application.

On the other hand, Pour does not teach a chip packaging in which the package substrate is connected to a first voltage and a first lead frame is connected to a second voltage that is the logical opposite of the first voltage.

New claims 28 and 31 are duplicates of original claims 13 and 21, and specify that the high voltage is obtained from a power supply and that the low voltage is ground.

New claims 29 and 32 are added to specify the case in which the package substrate is connected to a power supply and the first lead frame is connected to ground.

No new matter is added through any of the new claims 27-32, and acceptance of claims 27-32 is respectfully requested.

Respectfully submitted,

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